Training:
Failure Analysis and Reliability Challenges for Advanced Semiconductor Technologies

MIMOS Berhad, Technology Park Malaysia
25 -26 Mar 2019

Electronics are continuously growing more intricate, and are being integrated into ever more mission critical applications such as autonomous vehicles, avionics, and implantable devices that literally sustain patients' lives. Failure of any electronic device in these applications can cost millions of dollars, as well as result in loss of life. Even in devices where failures are not life threatening, customers' expectations place stringent demands on product requirements. No one wants a product to fail within its expected lifetime. Failures during qualifications can delay product launches; failures early in a product's lifetime can result in warranty costs that destroy profitability, and after-warranty failures can sour a customer's esteem for a company, ruining brand loyalty and destroying repeat business.

The training will show multiple examples of failure mechanisms and solutions taken from traditional and new package styles such as FC-BGAs, WCSPs, and the newest fan-out and through silicon via technologies. Throughout, the emphasis will be on using this information to eliminate future problems.

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LEARNING OUTCOMES

- Participants will know how to identify and solve reliability issues in both current and future package technologies, speeding time to market and increasing package development efficiency.

- Participants will understand good failure analysis procedures and techniques to eliminate "failure not found" and false failure findings. They will be able to help guide failure diagnostic journeys to give their companies a competitive advantage over others.

- Participants will be able to properly analyse and interpret reliability data, having a good understanding of statistical significance and common reliability charts. They will know the variables to control to ensure their products remain reliable.

- The described structured approach to risk elimination in new products will reduce wasted efforts, failed qualifications, field failures, and will result in faster time to market.

- An intuitive understanding of the interplay between materials, stresses, environmental conditions and reliability will help the student solve real-world problems for years to come.

METHODOLOGY

- This Course will utilise a combination of lecture and discussions
- Instructor led Classroom training

TARGET GROUP

This course is designed for Quality Control Engineer, Reliability Engineer and Failure Analysis Engineer, Packaging Engineer, Process and Materials Engineer, Also researchers from Academic sector

PRE-REQUISITE:

Diploma, BSc in EE, or 1-2 years working experience in semiconductor industry is an added advantage.

DAY 1

- Motivation
  - Reliability Nightmares and Their Causes
  - Upfront Development vs Band-aid Approaches
- Fundamentals of Reliability
  - Bathtub Curve
  - Acceleration Factors
  - Sample Sizes and Confidence Limits
  - The Weibull Distribution
  - Cp and Cpk
  - Trend Charts
- Failure Analysis
  - Failure Flow for Fault Isolation
  - Non-Destructive Methods: SAM, X-ray, 3D-X-ray, Optical Inspection, Witness Marks
  - Destructive FA: Cross Sectioning, Polish, Ion Mill, FIB, TEM, EDX

DAY 2

- Failure Mechanisms and Solutions by Package Type (a sampling)
  - Common Mechanisms: Scribe Seal Damage, Shear Stress Cracking, Finish Problems
  - FC-BGA: White Bumps, Bump Electromigration, Cu Pillar Reliability, Underfill Reliability, Substrate Failure Mechanisms (Trace Cracking, Via Cracking, Barrel Cracking, Cu Anodic Filament Shorts), Solder Joint Reliability (Temperature Cycling, Drop), Warpage Reliability Issues (Head-in-Pillow, Board Level Impact), Bend Test and Cratering, Black Pad
  - Molded & Leaded Package: Moisture Sensitivity, Wire Bond Reliability, Delamination and Wire Bonds (Stitch, Pad), Cu vs Al Wire Bond Reliability, Wire Sweep vs C Black Issues
  - WLCSP: Solder Joint Reliability, To Underfill or Not?, Die Strength
  - Embedded Die / Molded WLP: Delamination, Trace Cracking, Board Level Reliability
  - TSV: Micro Bump Reliability, Delamination, Cu Pumping
  - LEDs: Delamination, Yellowing
  - MEMS: Specific Requirements, Specialised Tests

- Adhesion Tests for Material Selection

- Reliability Tests and Standards
  - JEDEC, IPC, Mil Std
- Package Process Development
  - Materials Selection
  - Co-Design
  - Package Test Structures
  - Design Rules
  - Qualification By Similarity

- Q&A Session, End of Workshop

INSTRUCTOR PROFILE

Darvin R. Edwards received the B.S. degree in Physics from Arizona State University, Tempe, AZ, in 1980 and joined Texas Instruments soon after. Initially at TI, he developed integrated test structures such as strain gauges, moisture sensors, thermal sensors, and structures to determine the impact of package stresses on IC thin film layers. He developed a set of IC design rules for packaging that has been continuously updated and is still in use today. He then worked to build TI's competence in thermal characterisation and thermal management. He wrote a thermal characterisation modelling program that was used within TI from 1993 through 2004 and built TI's thermal labs. With JEDEC, he wrote the thermal test board standards.

Elected TI Fellow in 1999, he was a manager of the Advanced Package Modelling and Characterisation group from 1997 through 2012. His modelling team was responsible for thermal, electrical, and stress analysis for a wide range of product families, as well as ensuring reliability, successful qualification and introduction of products to the market. Packages and technologies he has helped develop include TSV, POP, Cu Pillar, Stacked Die, MCM, FC-BGA, PBGA, QFN, CSP, WLCSP, QFP, LOC, multi-die QFP, and SOICs.

In 2013, Darvin took responsibility for Analog Chip/Package Codesign, developing innovative test structures and reliability design guidelines for TI's new analog process nodes, including those of high voltage components. Additionally, he created and codified a risk assessment process that was implemented worldwide for TI's new package development projects. During his career at TI, Darvin also managed at various times advanced package FA technique development, adhesion characterisation development, and Sun Flip-Chip microprocessor package development.

REGISTRATION FORM Failure Analysis and Reliability Challenges for Advanced Semiconductor Technologies

MIMOS @ Technology Park Malaysia   25 -26 March 2019 (early bird 15 March 2019),

Please complete this form and fax or email to us

COURSE FEE	Fee per participant	Fee inclusive SST	
☐ Standard Registration	RM2,900.00	RM3,074.00	**HRDF** MALAYSIA *Claimable under HRDF Scheme–SBL*
☐ Early Bird Registration	RM2,700.00	RM2,862.00	
☐ Group Discount	RM2,500.00	RM2,650.00	
☐ Universities & Colleges	RM1,500.00	RM1,590.00	

No	PARTICIPANT DETAILS	CONTACT INFORMATION	MEAL PREFERENCE
1	Name: Designation:	Email: Mobile No.:	☐ Vegetarian ☐ Non-Vegetarian
2	Name: Designation:	Email: Mobile No.:	☐ Vegetarian ☐ Non-Vegetarian
3	Name: Designation:	Email: Mobile No.:	☐ Vegetarian ☐ Non-Vegetarian
4	Name: Designation:	Email: Mobile No.:	☐ Vegetarian ☐ Non-Vegetarian
5	Name: Designation:	Email: Mobile No.:	☐ Vegetarian ☐ Non-Vegetarian

Organisation : ....

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Contact Person : .... **Position** : ....

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AUTHORISATION

I understand and agree to MIMOS Berhad terms and conditions
(Signatory must be authorised to sign on behalf of the Organisation)

Signature and Company Stamp:

Name of the Authorised Person : ....

Position : .... **Date** : ....

Terms & Conditions:

1. Upon received of this registration form (MIMOS), we will invoice to the contact-person for payment processing.
2. Payment is required within 30 days upon receipt of the invoice. All payment must be received 7 working days prior to the training date. The fee shall include luncheon, coffee/tea breaks and training materials.
3. Cancellation or postponement – Any cancellation must be made in writing and to reach us no later than 10 working days prior to the training date. If written notice is received in less than 10 working days, 100% of total fees is chargeable. A substitute delegate with similar background and competencies, is always welcome at no additional charge.
4. Our instructor(s) and topics are confirmed at the time of this print. However, circumstances beyond the control of the organisers' may occur and MIMOS Berhad reserves the rights to alter or modify the advertised speakers/ topics if necessary.

To register & more information:

Business Development (MSSB), MIMOS Berhad

Call : +603-8995 5000 ext. 55279 (Fara), 55642 (Amy)   Email : faradaya.machmud@mimos.my, letchumy@mimos.my