Design and Verification of Low Voltage Low Power Dynamic Comparator over PVT Variation

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***Abstract*— This paper presents a low voltage low power dynamic comparator with 45 process corners verification. In 45 process corner simulation, circuit is simulated with 10% voltage supply variation, five process corners FF, SS, TT, FS, SF variation and temperature variation in between 0°C to 100°C. The comparator is simulated in 0.18µm CMOS technology with supply voltage 0.8 volt using Virtuoso Cadence tool. From simulated result, significant improvement on power consumption and delay is achieved during worst case condition. Details on verification method are presented in this paper.**

Keywords— dynamic comparator; double-tail dynamic comparator; low power comparator; ADC; SAR ADC.

I. INTRODUCTION

Low power and high speed are the main criteria in designing comparator for Successive Approximation Register Analog to Digital converter (SAR ADC). According to Walden figure of merit (FOM), the state-of-the-art for SAR ADC is reduced to below than 1 fJ per conversion step. However, comparator is not scaled in the same direction with supply voltage and technology. Besides, it consumes 50-60% energy from SAR ADC circuit [1,5]. Thus, the need for low power low voltage comparator for SAR ADC is crucial. In SAR ADC, comparator is the main block for converting analog voltage to digital logic. The comparator circuit needs to be robust enough to operate in critical condition. To verify the robustness of fabricated comparator circuit design, process corner simulation is required at the design stage. Process corner represents the extremes parameter variation of integrated circuit design which fabricated in semiconductor wafer. Parameter variations including range of process transistor properties, supply voltages and die temperatures.

The most popular energy efficient comparator is dynamic comparator (Fig. 1) which only operates during regeneration time [2,3,5]. The additional features are high input impedance, rail to rail output swing, zero static power, low offset voltage and fast decision making that comes from strong positive feedback and differential input architecture [1,7]. However, this topology requires high supply voltage to operate the circuit because of high numbers of transistors stacking. For this reason, this topology is perceived to be unsuitable for ultra-dep sub-micrometer CMOS technology with limited supply voltage and small voltage headroom.

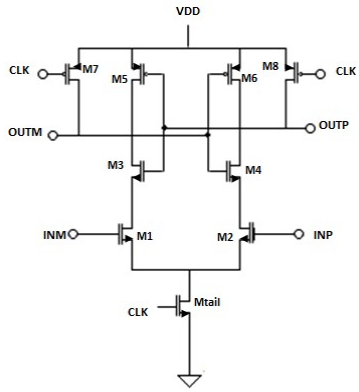

Fig. 1. Schematic diagram of the conventional dynamic comparator

In double-tail dynamic comparator proposed by *Schinkel 2007*, number of stacking transistor was reduced by splitting pre-amplifier and latching stage. In directly, the isolation between input and output node improves the kickback noise [1,3]. However, this topology consumes high power consumption because of pre-amp and latching stage operate at the same duration [1]. Further, the two phase latching clock method also contributes to high energy consumption, large die area and increase delay at regeneration time [4].