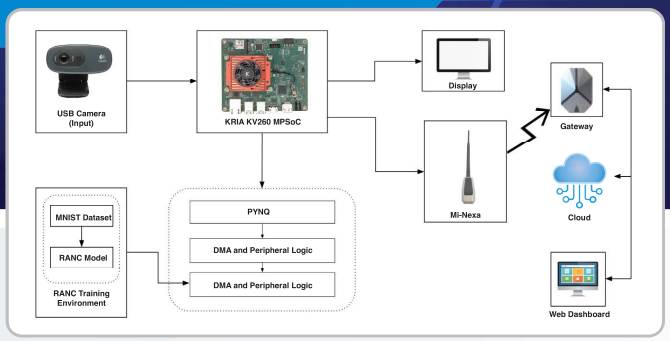
Neuromorphic and FPGA for Edge AI

The Neuromorphic and FPGA for Edge AI project explores the ground-breaking potential of Neuromorphic Computing in Edge AI (Artificial Intelligence) applications. Neuromorphic Computing represents a paradigm shift in computational methods, drawing inspiration from the human brain's functioning to deliver energy-efficient and adaptive AI solutions. At the core of this initiative is the Reconfigurable Architecture for Neuromorphic Computing (RANC), a cutting-edge concept poised to transform AI processing.



Technology Overview

Neuromorphic computing combined with FPGA acceleration enables energy-efficient, scalable, and adaptive AI at the edge. Leveraging the Kria KV260 MPSoC and a neuromorphic IP core, spiking neural networks (SNNs) are implemented for efficient pattern recognition, low-power operation, and real-time processing.

A demonstration highlights handwritten digit classification using the MNIST dataset, streamed from a USB camera to the FPGA and displayed in real time. Classification results are transmitted via the Mi-Nexa (6LoWPAN) wireless protocol to a gateway and visualised on a cloud dashboard. This proof-of-concept illustrates the versatility and real-world applicability of scalable neuromorphic edge AI across broader domains.

Key Features

- **Low Power Consumption**
  The neuromorphic architecture mimics the human brain's energy efficiency, making it well-suited for battery-powered or remote applications. An MNIST demonstration highlights how the technology can classify data with minimal power usage.
- **Real-Time Processing**
  FPGA technology enables instant inference, crucial for latency-sensitive applications. The demo unit enables instant digit recognition directly from the camera input, demonstrating its real-time capability.
- **Wireless Connectivity**
  The demo unit transmits classification results wirelessly to a gateway and cloud dashboard. This feature demonstrates how the system can communicate efficiently with other devices and monitoring platforms.
- **Integrated Simulation & Deployment**
  Models are trained and tested in the RANC simulator, then deployed seamlessly to FPGA hardware.
- **Adaptive & Scalable Design**
  Architecture can be scaled from simple digit recognition to more complex AI tasks such as license plate or biosensor data analysis.

Technology Benefits

- **Efficiency**
  By mimicking the brain's parallel processing, the system performs tasks like digit recognition with a fraction of the energy of traditional computing methods (CPUs/GPUs).
- **Adaptability**
  The technology learns to recognise different pattern. For instance, the system can be trained to recognise a variety of handwritten styles, showcasing its ability to adapt to data variations.
- **Scalability**
  The underlying architecture can be efficiently scaled from simple tasks like digit classification to large-scale, complex problems without compromising performance.

Applications

- **Healthcare**
  Real-time analysis of medical data, such as classifying and detecting anomalies in EEG data from wearable devices.
- **Industrial Automation**
  Adaptive control systems for robotics and smart factories that use real-time visual inspection, similar to how our system recognises patterns in digits.
- **License Plate Recognition**
  Neuromorphic-based vision systems detect and classify numbers on license plates in real time for traffic monitoring and security, operating with less power than conventional systems.

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